Order this document by MC3487/D

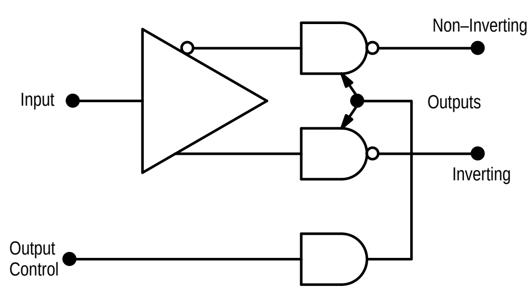
MOTOROLA

Quad Line Driver with Three-State Outputs

Motorola's Quad EIA–422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three–state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

- Four Independent Driver Chains
- Three–State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typical 15 ns)
- TTL Compatible
- Single 5.0 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- DS 3487 Provides Second Source

Driver Block Diagram



TRUTH TABLE

Input	Control Input	Non–Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

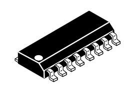
L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third–State (High Impedance)

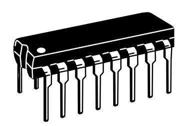
MC3487

QUAD EIA–422 LINE DRIVER WITH THREE–STATE OUTPUTS

SEMICONDUCTOR TECHNICAL DATA

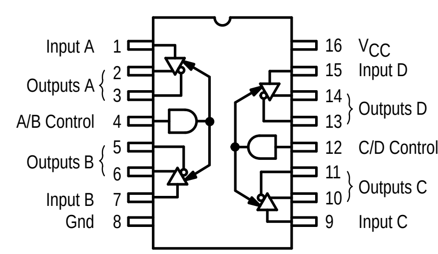
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)





P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3487P	T_A = 0 to +70°C	Plastic DIP
MC3487D		SO–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J	150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V and 0°C $\leqslant T_A \leqslant$ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State (V_{IL} = 0.5 V)	I_{IL}	–	–	– 400	µA
Input Current – High Logic State (V_{IH} = 2.7 V) (V_{IH} = 5.5 V)	I_{IH}	 – –	 – –	 + 50 + 100	µA
Input Clamp Voltage (I_{IK} = –18 mA)	V_{IK}	–	–	– 1.5	V
Output Voltage – Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State (I_{OH} = –20 mA)	V_{OH}	2.5	–	–	V
Output Short–Circuit Current (V_{IH} = 2.0 V, Note 1)	I_{OS}	– 40	–	– 140	mA
Output Leakage Current – Hi–Z State (V_{IL} = 0.5 V, $V_{IL(Z)}$ = 0.8 V) (V_{IH} = 2.7 V, $V_{IL(Z)}$ = 0.8 V)	$I_{OL(Z)}$	 – –	 – –	 ± 100 ± 100	µA
Output Leakage Current – Power OFF (V_{OH} = 6.0 V, V_{CC} = 0 V) (V_{OL} = –0.25 V, V_{CC} = 0 V)	$I_{OL(off)}$	 – –	 – –	 + 100 – 100	µA
Output Offset Voltage Difference (Note 2)	$V_{OS} - \overline{V}_{OS}$	–	–	± 0.4	V
Output Differential Voltage (Note 2)	V_{OD}	2.0	–	–	V
Output Differential Voltage Difference (Note 2)	$\lvert \Delta V_{OD} \rvert$	–	–	± 0.4	V
Power Supply Current (Control Pins = Gnd, Note 3) (Control Pins = 2.0 V)	 I_{CCX} I_{CC}	 – –	 – –	 105 85	mA

NOTES: 1. Only one output may be shorted at a time.
2. See EIA Specification EIA–422 for exact test conditions.
3. Circuit in three–state condition.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times High to Low Output Low to High Output	 t_{PHL} t_{PLH}	 – –	 – –	 20 20	ns
Output Transition Times – Differential High to Low Output Low to High Output	 t_{THL} t_{TLH}	 – –	 – –	 20 20	ns
Propagation Delay – Control to Output (R_L = 200 Ω, C_L = 50 pF) (R_L = 200 Ω, C_L = 50 pF) (R_L = ∞, C_L = 50 pF) (R_L = 200 Ω, C_L = 50 pF)	 $t_{PHZ(E)}$ $t_{PLZ(E)}$ $t_{PZH(E)}$ $t_{PZL(E)}$	 – – – –	 – – – –	 25 25 30 30	ns

Figure 1. Three–State Enable Test Circuit and Waveforms

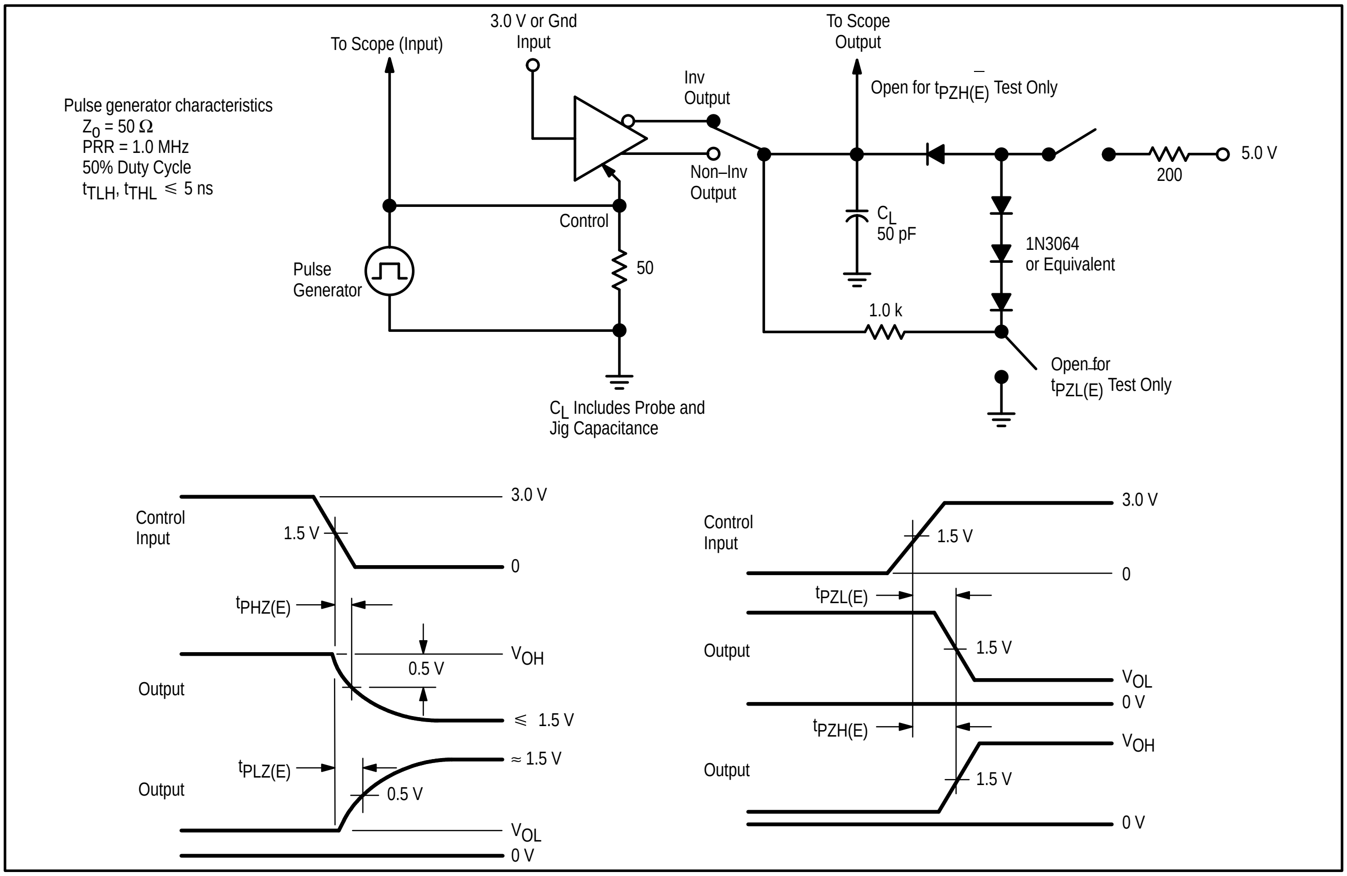


Figure 2. Propagation Delay Times Input to Output Waveforms and Test Circuit

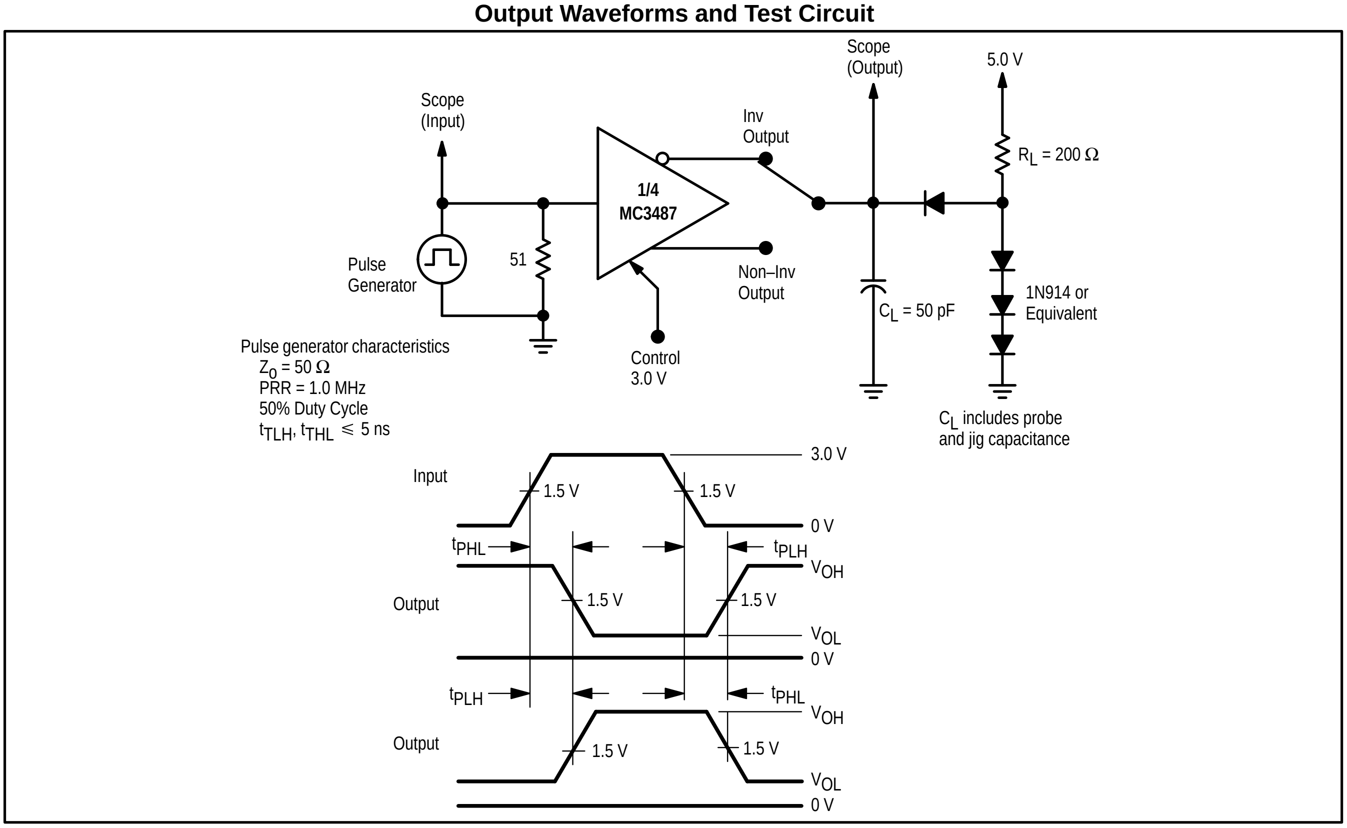


Figure 3. Output Transition Times Test Circuit and Waveforms

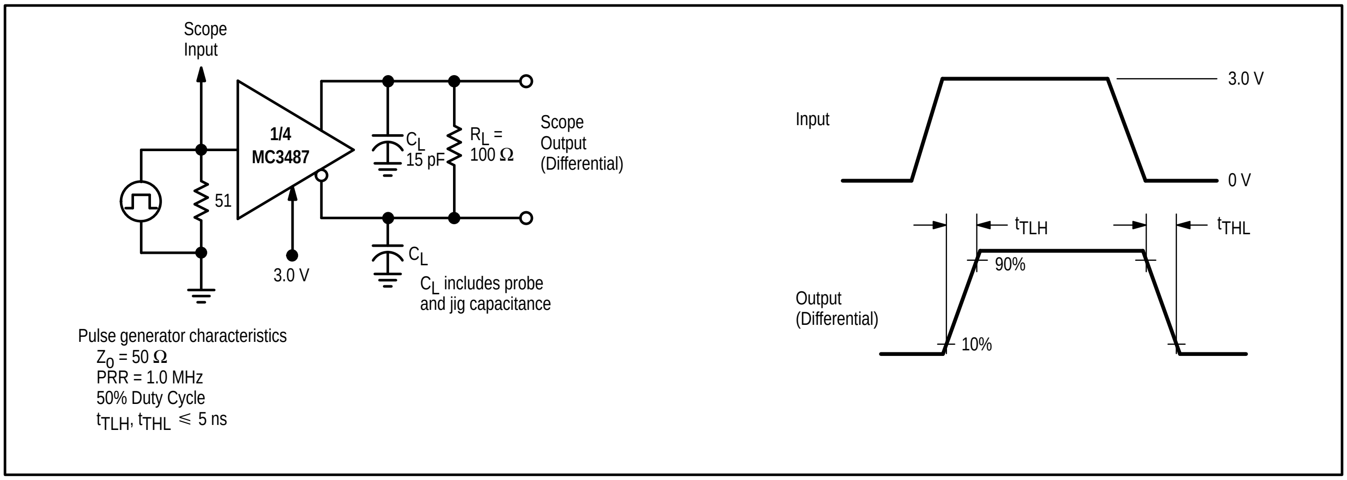


Figure 4. Output Current versus Output Voltage

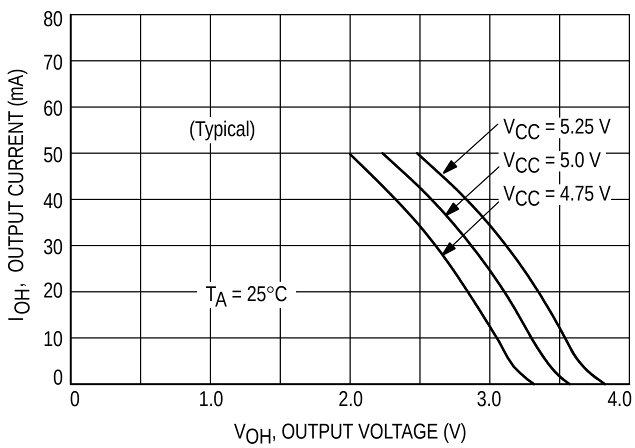
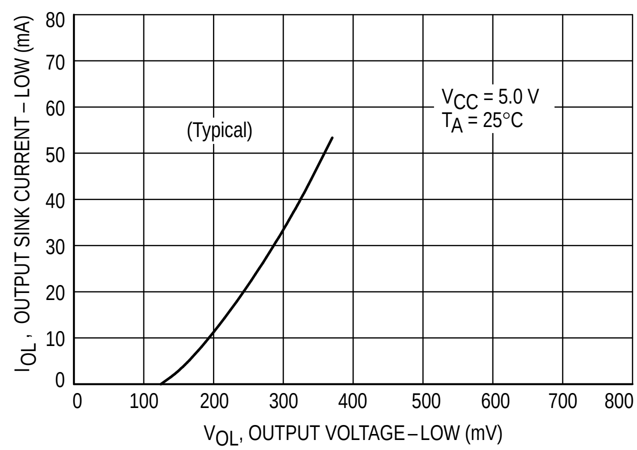
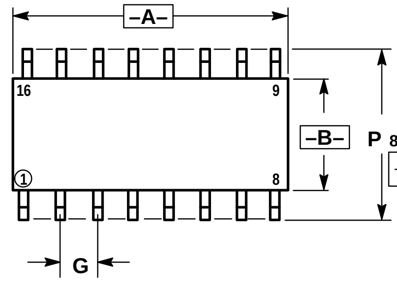


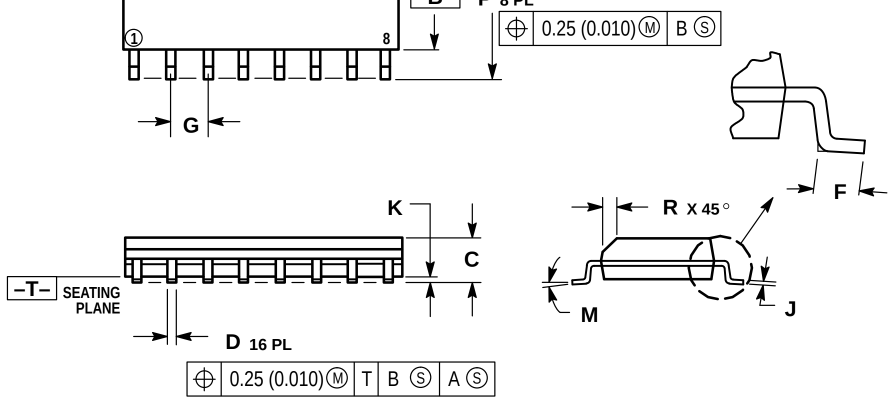
Figure 5. Output Sink Current versus Output Voltage



OUTLINE DIMENSIONS

D SUFFIX
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CASE 751B–05
(SO–16)
ISSUE J

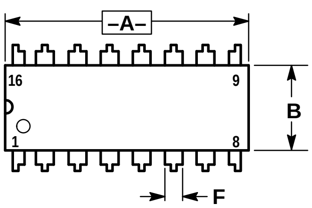


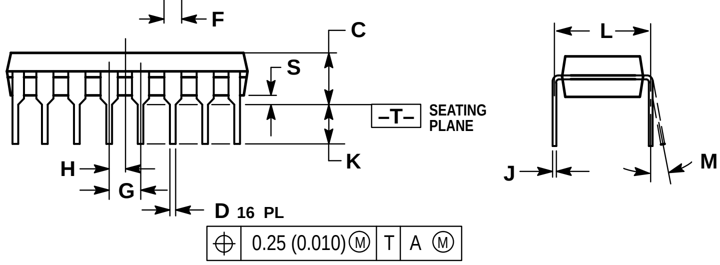


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

P SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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